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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,404	02/11/2002	Feng-Tso Chien	25740-02A	3989

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,404	CHIEN, FENG-TSO	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant has amended claims 1 and 3 to read are around the prior art of record from the previous office action filed on 2/13/03. Claims 1 and 3 will be further examined.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the P+ well between the N- epitaxial layer and P- well interface must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. The currently the drawings only show the P+ well partially between the N- epitaxial and the P- well interface, but not completely as one having skill in the art would interpret in claims 1 and 3.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0177277 Baliga.

3. Referring to claim 1, a power MOSFET device with reduced snap-back and being capable of increasing avalanche-breakdown current endurance, which is sequentially a drain with N^{+} silicon substrate, (Figure 1 #100), an N^{-} epitaxial layer, (Figure 1 #102 and 130), formed on said N^{+} silicon substrate, (Figure 1 #100), a source contact region formed of a N^{+} doped well, (Figure 1 #133), and P^{+} doped well, (Figure 1 #128), implanted after etching in a P^{-} well, (Figure 1 #126), formed on said N^{-} epitaxial layer, (Figure 1 #102 and 130), and a gate electrode, (Figure 1 #118), with deposition of polysilicon, (Paragraph 0056 Lines 35-37), above a channel region, (Figure 1 area of #130), between said N^{-} epitaxial layer, (Figure 1 #102 & 130), and N^{+} source contact region, (Figure 1 #133), said device is characterized in that: said source contact region, (Figure 1 #133), is formed by etching into said P^{-} well, (Figure 1 #126), first and implanting P^{+} dopant, (Figure 1 #128), to the interface between said N^{-} epitaxial layer, (Figure 1 #102 & 130), and P^{-} well, (Figure 1 #126), and the source contact region of said N^{+} well, (Figure 1 #133), and that of said P^{+} well, (Figure 1 #128), are not at the same level and are separated by at least a portion of the P- well, (Figure 1 #126), by which it is possible to increase the avalanche breakdown current durable capability of the power MOSFET device.

Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

4. Referring to claim 3, a power MOSFET device comprising: an N^+ silicon substrate, (Figure 1 #100); a gate electrode, (Figure 1 #118); an N^- epitaxial layer, (Figure 1 #102 & 130), formed above said N^+ silicon substrate, (Figure 1 #100), at least a portion of which is intermediate the N^+ silicon substrate, (Figure 1 #100), and the gate electrode, (Figure 1 #118); a P^- well, (Figure 1 #126), implanted in the N^+ well, (Figure 1 #133), implanted in the N^- epitaxial layer, (Figure 1 #102 & 130); a source contact region, (Figure 1 #133), etched into the P^- well, and formed of an N^+ doped well, (Figure 1 #133), and a P^+ well, (Figure 1 #128), wherein the P^+ doped well, (Figure 1 #128), interfaces the N^- epitaxial layer, (Figure 1 #102 & 130), and the P^- well, (Figure 1 #126), and the N^+ doped well, (Figure 1 #133), is located above the P+ doped well, (Figure 1 #128), and separated from the P+ doped well, (Figure 1 #128), by at least a portion of the P- well, (Figure 1 #126); whereby the snap back is reduced and the avalanche breakdown current endurance is increased.

Initially, and with respect to claim 3, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ

11/15/03